



Form PTO-1449 <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b> (Use several sheets if necessary)	Docket Number 416272004201	Application Number 10/729,726
	Applicant Sung-Mo KANG and Seung-Moon YOO	
	Filing Date December 5, 2003	Group Art Unit 2838 <b>2816</b>
	Mailing Date April 5, 2004	

## U.S. PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Name	Class	Subclass	Filing Date If Appropriate
JZ	1.	5/19/1992	5,115,150	Ludwig, Mark A.	—	—	
<i>see PTO-892</i>	2.	<del>9/29/1992</del>	<del>5,151,620</del>	<del>Lin, Ming-Zen</del>	—	—	
JZ	3.	12/29/1992	5,175,448	Fujii	—	—	
JZ	4.	8/26/1997	5,661,419	Bhagwan	—	—	
892	5.	<del>3/9/1999</del>	<del>5,880,604</del>	<del>Kawahara et al.</del>	—	—	
<i>see PTO-892</i>	6.	<del>4/11/2000</del>	<del>6,049,245</del>	<del>Son et al.</del>	—	—	
892	7.	<del>8/22/2000</del>	<del>6,107,869</del>	<del>Horiguchi et al.</del>	—	—	
892	8.	<del>2/20/2001</del>	<del>6,191,615</del>	<del>Koga, Hiroshi</del>	—	—	
JZ	9.	3/20/2001	6,204,696	Krishnamurthy et al.	—	—	
JZ	10.	4/9/2002	6,370,052 B1	Hsu et al.	—	—	
892	11.	<del>6/11/2002</del>	<del>6,404,269</del>	<del>Voldman</del>	—	—	
892	12.	<del>6/25/2002</del>	<del>6,411,157</del>	<del>Hsu et al.</del>	—	—	
JZ	13.	8/27/2002	6,442,086 B1	Dean	—	—	
JZ	14.	12/2002	6,492,837 B1	Narendra et al.	—	—	
JZ	15.	5/21/2002	10/153,158	Yoo et al.	—	—	

## FOREIGN PATENT DOCUMENTS

Examiner Initials	Ref. No.	Date	Document No.	Country	Class	Subclass	Translation YES NO

## OTHER DOCUMENTS

(including author, title, Date, Pertinent Pages, Etc.)

Examiner Initials	Ref. No.	Title
<i># JZ</i>	16.	M. Anis et al., "Dynamic and Leakage Power Reduction in MTCMOS Circuits Using an Automated Efficient Gate Clustering Technique", IEEE, June 10-14, 2002, New Orleans, Louisiana, pp. 480-485.
<i># JZ</i>	17.	Assaderaghi et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low

EXAMINER: *Jeffrey Zweizig*DATE CONSIDERED: *11/22/04*

EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

x- ~~Did not receive~~

<b>Form PTO-1449</b>  <b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <i>(Use several sheets if necessary)</i>	Docket Number 416272004201	Application Number 10/729,726
	Applicant Sung-Mo KANG and Seung-Moon YOO	
	Filing Date December 5, 2003	Group Art Unit 2838
	Mailing Date April 5, 2004	

cont		Voltage Operation", <i>International Electron Devices Meeting, Digest of Technical Papers</i> , pages 809-812, June 1994.
JZ	18.	J. Burr and J. Scott, "A 200mV Self-Testing Encoder/Decoder using Stanford Ultra-Low-Power CMOS", <i>ISSCC Digest of Technical Papers</i> , pages 84-85, February 1994.
JZ	19.	Mark N. Horenstein, <i>Microelectronic Circuits &amp; Devices</i> , 1996, pgs. 240-250.
JZ	20.	M. Horiguchi et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's", <i>IEEE Journal of Solid State Circuits</i> , 28(11):1131-1135, November 1993.
JZ	21.	T. Iwata et al., "Gate-Over-Driving CMOS Architecture for 0.5V Single-Power-Supply-Operated Devices", <i>ISSCC Digest of Technical Papers</i> , pages 290-291, February 1997.
JZ	22.	Kawaguchi et al., "A CMOS Scheme for 0.5V Supply Voltage with Pico-Ampere Standby Current", <i>ISSCC Digest of Technical Papers</i> , pages 192-193, February 1998.
JZ	23.	T. Kuroda et al., "A 0.9V 150MHz 10mW 4mm <sup>2</sup> 2D Discrete Cosine Transform Core Processor with Variable-Threshold-Voltage Scheme", <i>ISSCC Digest of Technical Papers</i> , pages 166-167, February 1996.
JZ	24.	Mutoh et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", <i>IEEE Journal of Solid State Circuits</i> , 30(8): 845-854, August 1995.
JZ	25.	K. Seta et al., "50% Active-Power Saving without Speed Degradation Using Standby Power Reduction (SPR) Circuit", in <i>ISSCC Digest of Technical Papers</i> , pages 318-319, February 1995.
JZ	26.	S. Shigematsu et al., "A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits", <i>IEEE Journal of Solid State Circuits</i> , 32(6):861-869, June 1997.
JZ	27.	Seung-Moon Yoo et al., "New High Performance Sub-1V Circuit Technique with Reduced Standby Current and Robust Data Holding", <i>IEEE International Symposium on Circuits and Systems</i> , May 28-31, 2000, Geneva, Switzerland (Pages 1-4)
considered but	28.	<del>Notice of Allowance and Fee due, Notice of Allowability and Examiner's Amendment for Application Ser. no. 10/153,158, 6 pgs.</del>
not printed	29.	<del>Amendment A for the U. S. patent application 10/153,158, Yoo et al., filed 5/21/2002, 13 pgs. 4/9/2003.</del>
JZ	30.	International Search Report mailed on February 25, 2004, for PCT/US03/24976 filed on August 8, 2003, 7 pgs.

~~Did not receive~~

EXAMINER: Jeffrey Z weizig	DATE CONSIDERED: 11/22/04
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ALTERNATIVE TO PTO/SB/06a/b (08-03)

Substitute for form 1449/PTD				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				Application Number	10/729,726
				Filing Date	December 5, 2003
				First Named Inventor	Sung-Mo KANG
				Art Unit	2816
				Examiner Name	J. S. Zweizig
Sheet	1	of	1	Attorney Docket Number	416272004201

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.*	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JZ	1.	6,759,873	7/6/2004	Kang et al.	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.*	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Country Code <sup>2</sup>	Number-Kind Code <sup>2</sup> (if known)				

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>4</sup>

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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	Jeffrey Zweizig	Date Considered	11/22/04
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